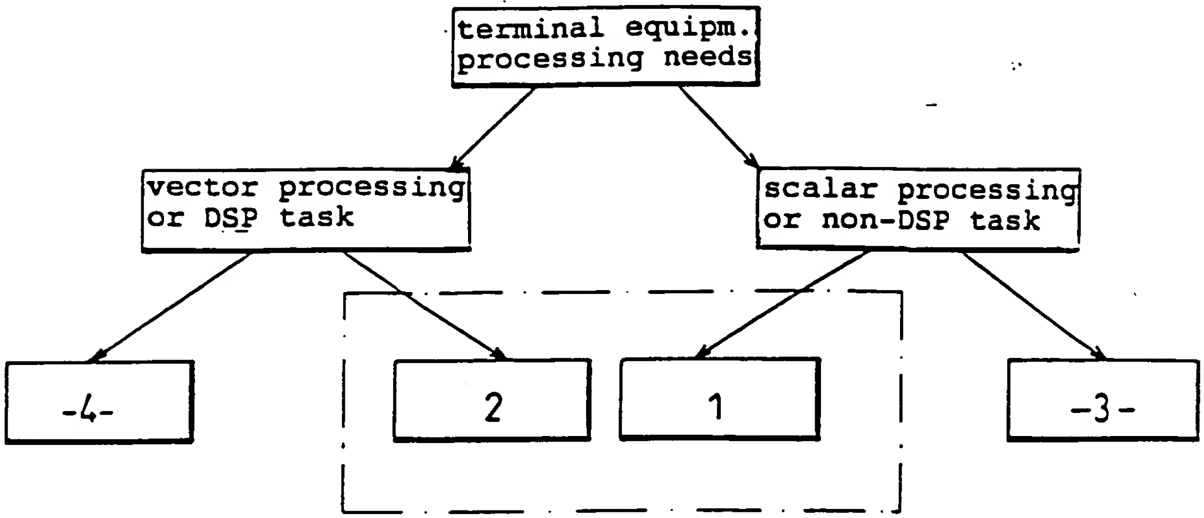
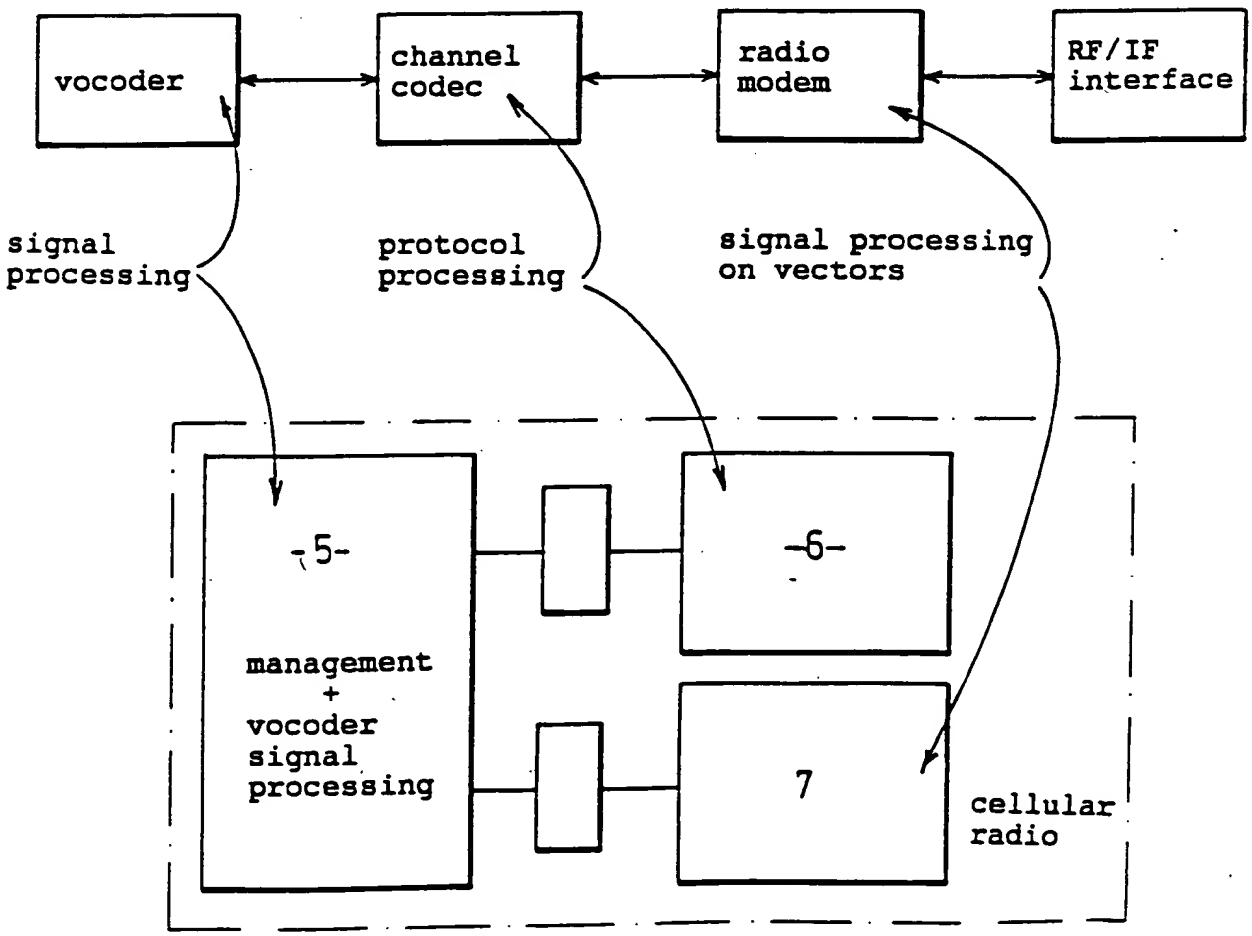

terminal equipm.
processing needs
vector processing
or DSP task
scalar processing
or non-DSP task
-4-
2
1
-3-

FIG·1


vocoder
channel
codec
radio
modem
RF/IF
interface
signal
processing
protocol
processing
signal processing
on vectors
-5-
management
+
vocoder
signal
processing
-6-
7
cellular
radio

FIG·2

PERFORMANCE OF CHANNEL CODEC ROUTINES

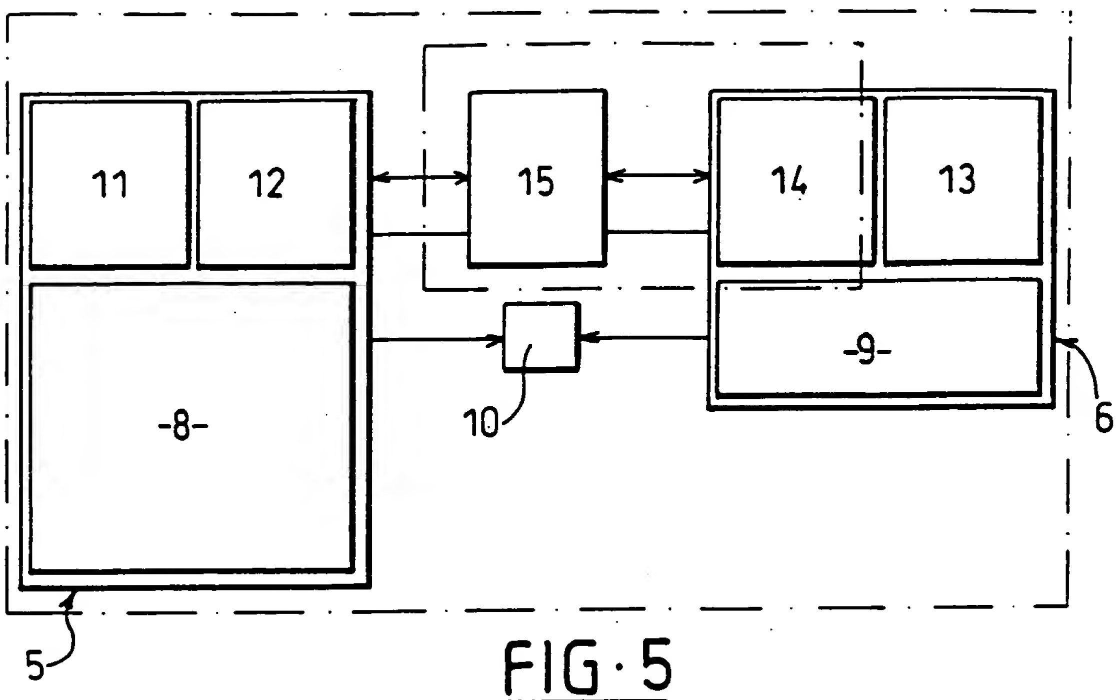
routines	DSP C5x utilisation	proc. protocol PP utilisation
16 bit CRC identification	6 instr/ bit 5 instr/bit	4 instr/bit 1 instr/ bit
RATIO		
sel/instr efficiency no. of trans. MIPS	×1 58 KTx 28 MIPS	×2,2 6,5 KTx 28×2,2=62 MIPS DSP

FIG·3

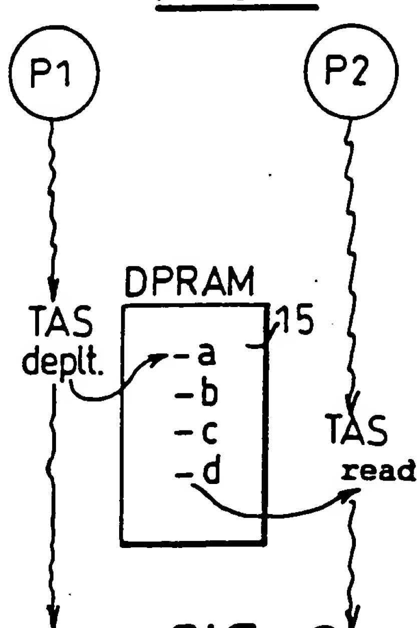
PERFORMANCE OF MODEM ROUTINES

routines	DSP C5x utilisation	array proc.
metric computation 57 symbols (4 samples)	43800 cycles	4400 cycles
RATIO		
instruction setting efficiency MIPS	×1 28 MIPS	×10 28×10=280 MIPS DSP

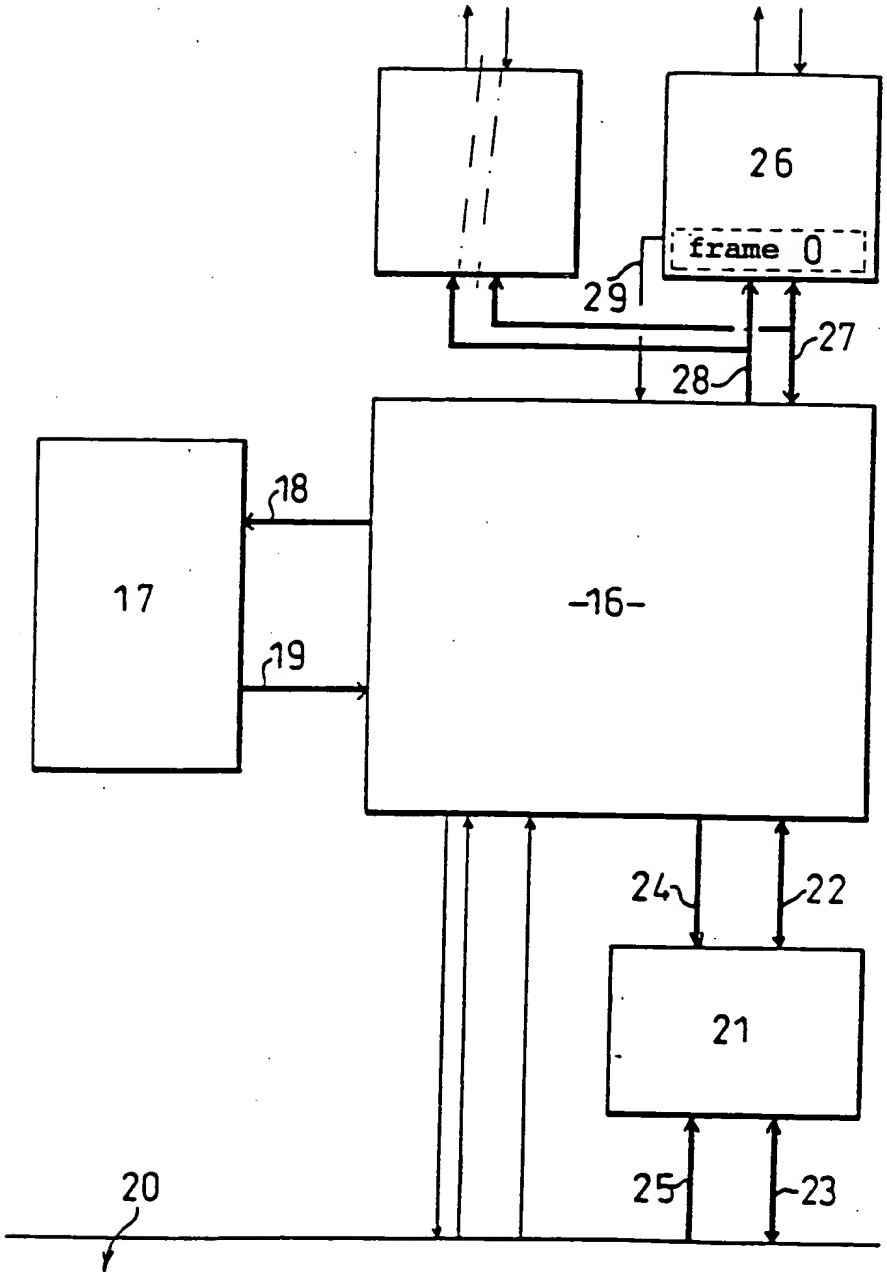
FIG·4



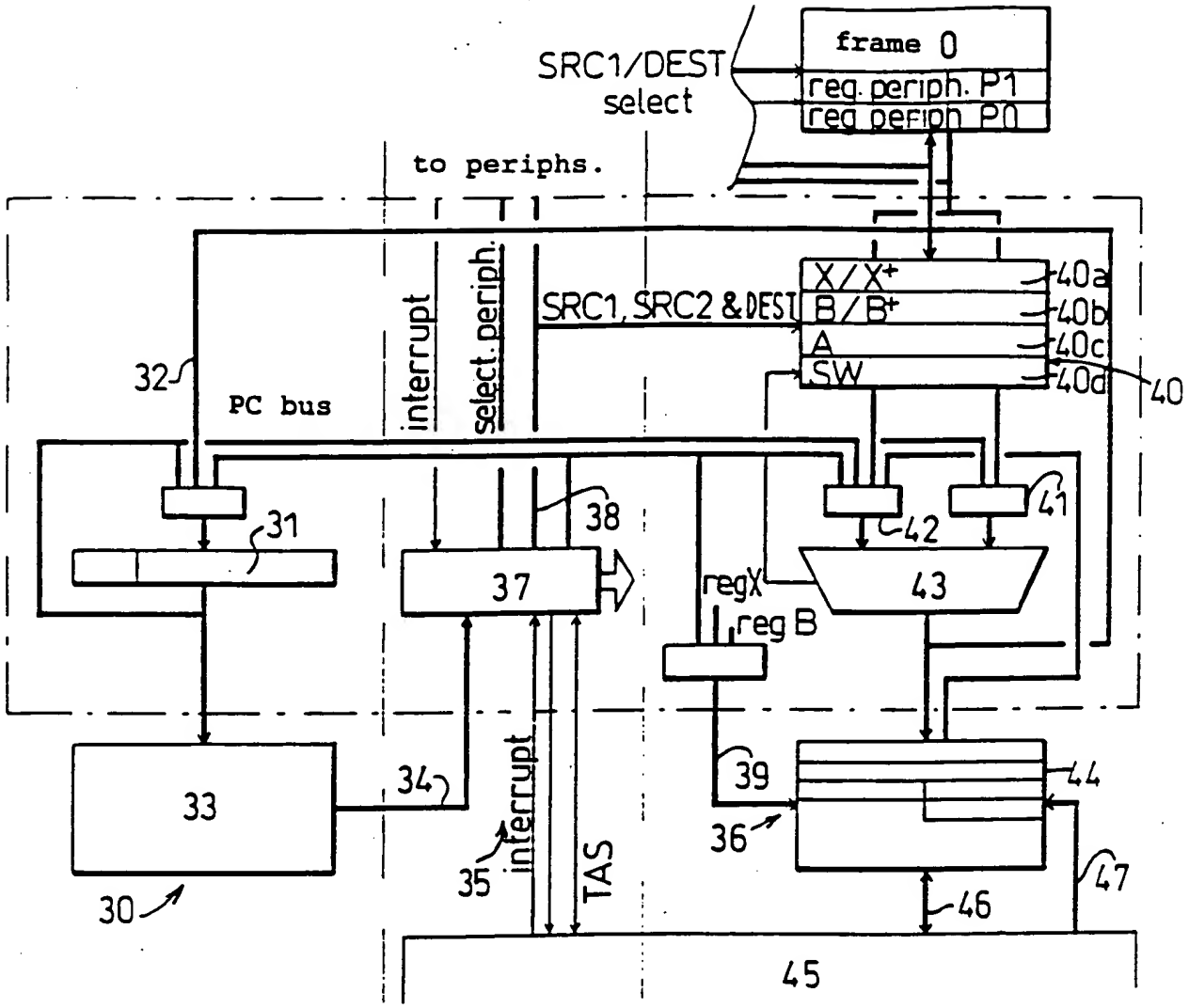
FIG·5



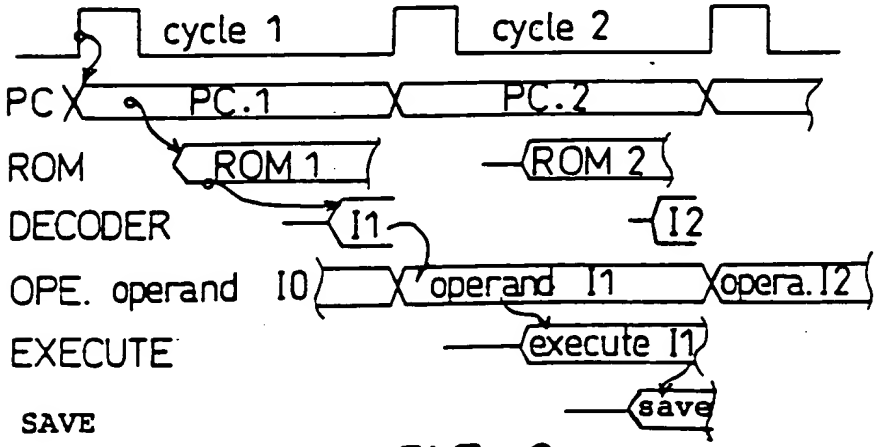
FIG·6



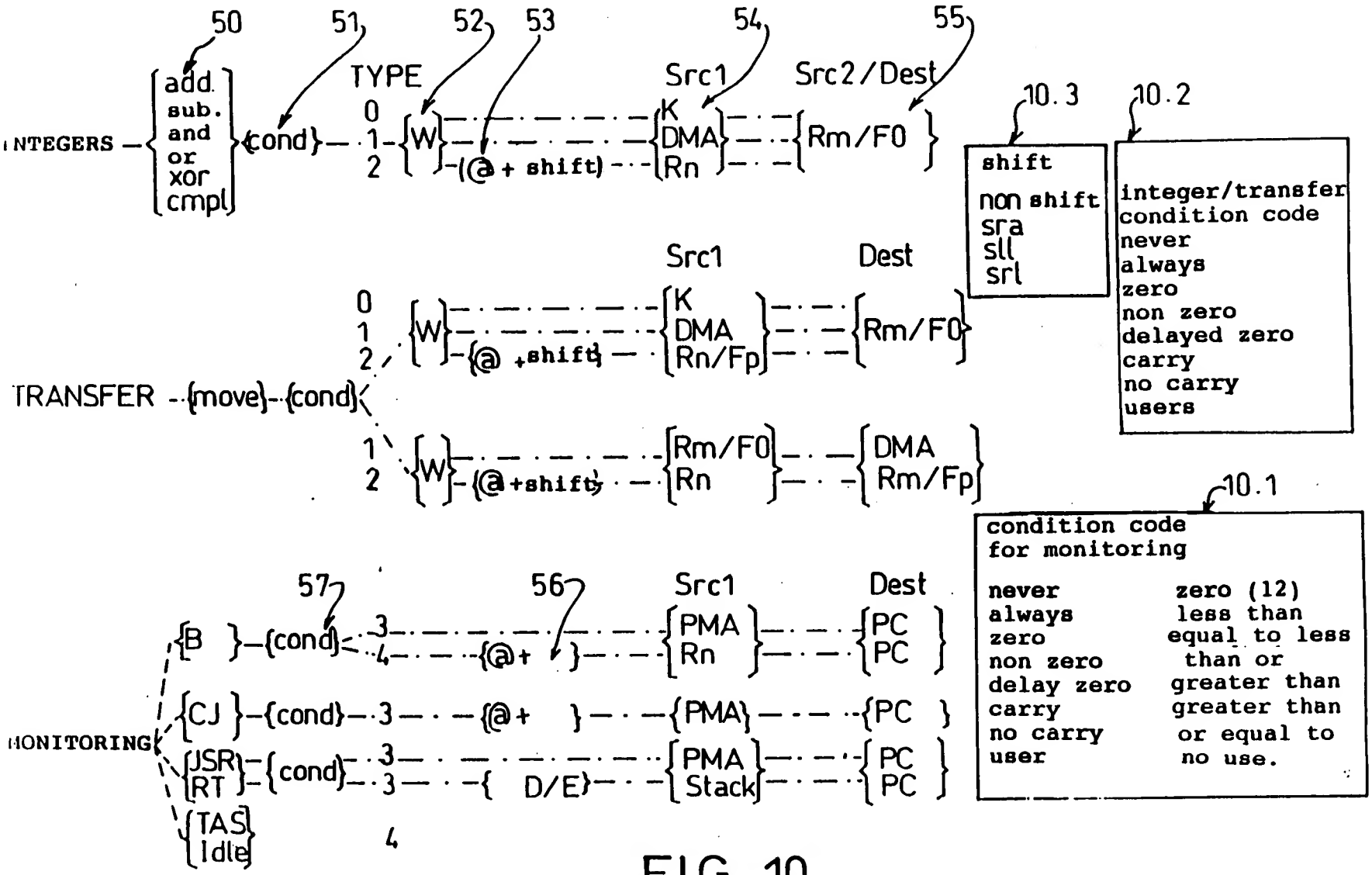
FIG·7


frame 0
SRC1/DEST select
reg. periph. P1
reg. periph P0
to periphs.
X/X+
B/B+
A
SW
40a
40b
40c
40d
40
SRC1, SRC2 & DEST
interrupt
select. periph.
32
PC bus
31
38
37
41
42
43
regX
reg B
33
34
39
44
36
35
interrupt
TAS
47
46
30
45

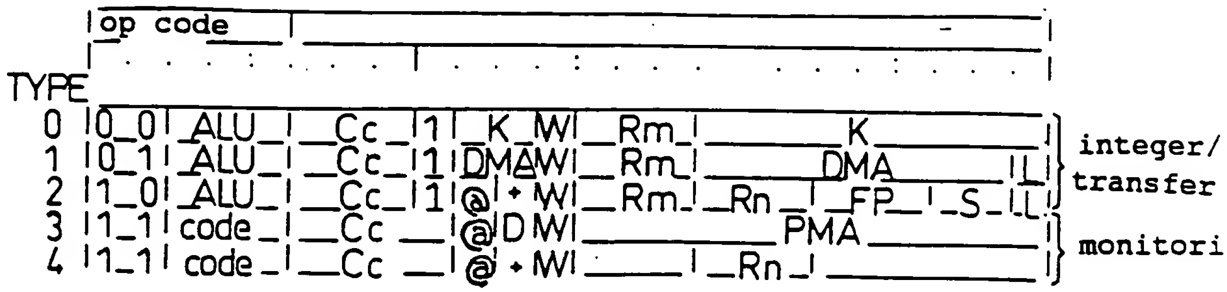
FIG·8


cycle 1
cycle 2
PC
PC.1
PC.2
ROM
ROM 1
ROM 2
DECODER
I1
I2
OPE. operand
I0
operand I1
opera. I2
EXECUTE
execute I1
SAVE
save

FIG·9


50
51
52
53
54
55
TYPE
Src1
Src2/Dest
INTEGERS
add
sub.
and
or
xor
cmpl
{cond}
0
1
2
{W}
(@ + shift)
K
DMA
Rn
Rm/F0
10.3
shift
non shift
sra
sll
srl
10.2
integer/transfer
condition code
never
always
zero
non zero
delayed zero
carry
no carry
users
Src1
Dest
0
1
2
{W}
{@ +shift}
K
DMA
Rn/Fp
Rm/F0
TRANSFER
{move}
{cond}
1
2
{W}
{@+shift}
Rm/F0
Rn
DMA
Rm/Fp
10.1
condition code
for monitoring
never
always
zero
non zero
delay zero
carry
no carry
user
zero (12)
less than
equal to less
than or
greater than
greater than
or equal to
no use.
57
56
Src1
Dest
{B }
{cond}
3
4
{@+ }
PMA
Rn
PC
PC
MONITORING
{CJ }
{cond}
3
{@+ }
PMA
PC
{JSR}
{RT }
{cond}
3
3
{ D/E}
PMA
Stack
PC
PC
{TAS}
{Idle}
4

FIG·10



FIG·11

ALU

0 - sub
1 - CPL
2 - add
3 - and
4 - or
5 - XOR
6 - PASSA
7 - SUBC

Code

0 – ST type 1
1 - ST type 2
2 - B type 3
3 - B type 4
4 - CALL
5 - RTS
6 - RTI
7 - STOP

Cc

0 - never
1 - always
2 - Z
3 - NZ
4 - ZD
5 - C
6 - NC
7 - user
8 - Z12
9 - LO
10 - LE
11 - G
12 - GE
13 - NU
14 - (BL)
15 -

Rm/Rn

0 - PO
1 - P1
2 - A
3 - B
4 - X
5 - PC
6 - SW
7 - SP

W

0 - R/W byte
1 - R/W word

L

0 - Rm low
1 - Rm high

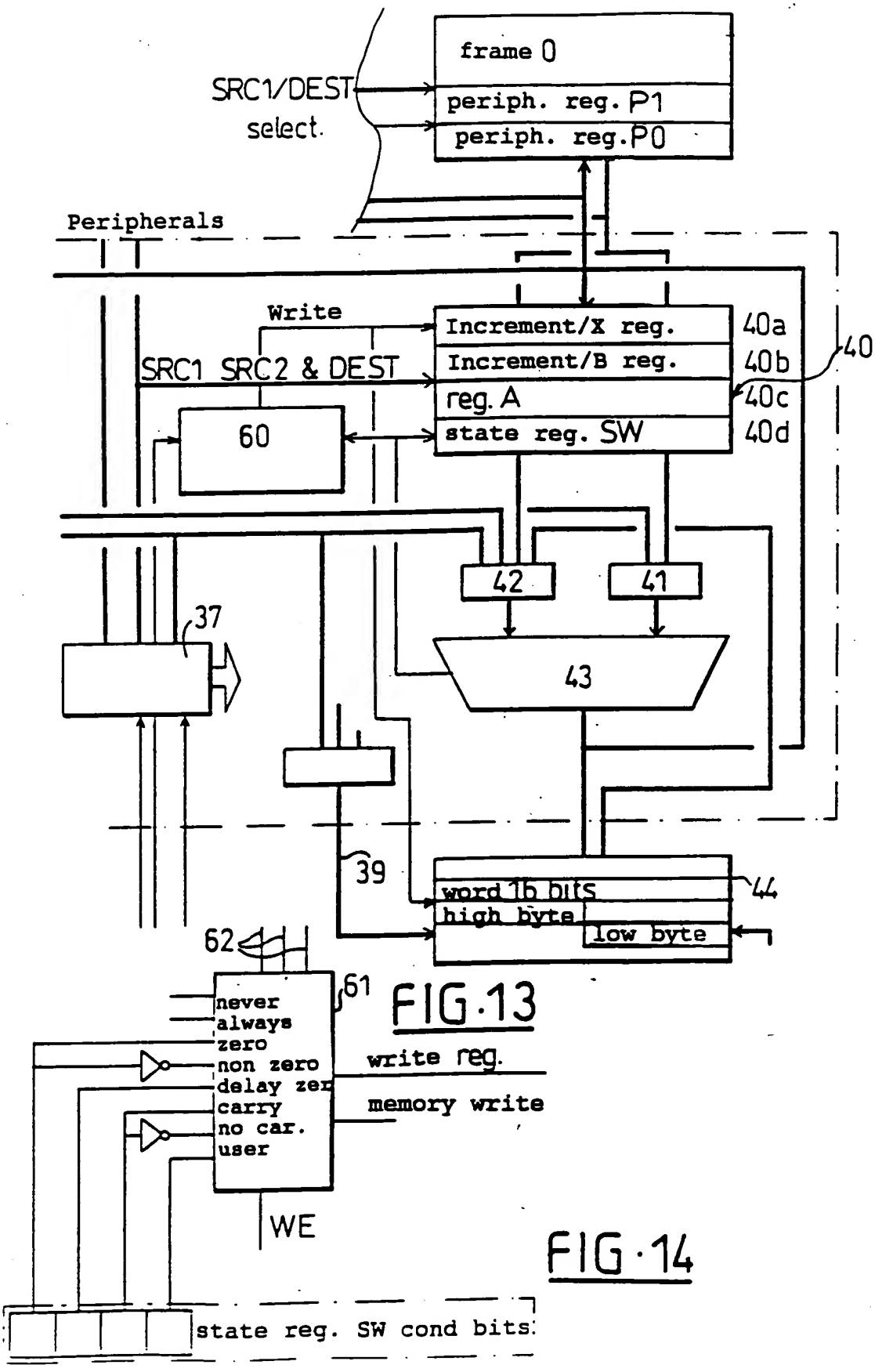
S

0 - PASS
1 - SRA
2 - SLL
3 - SRL

L

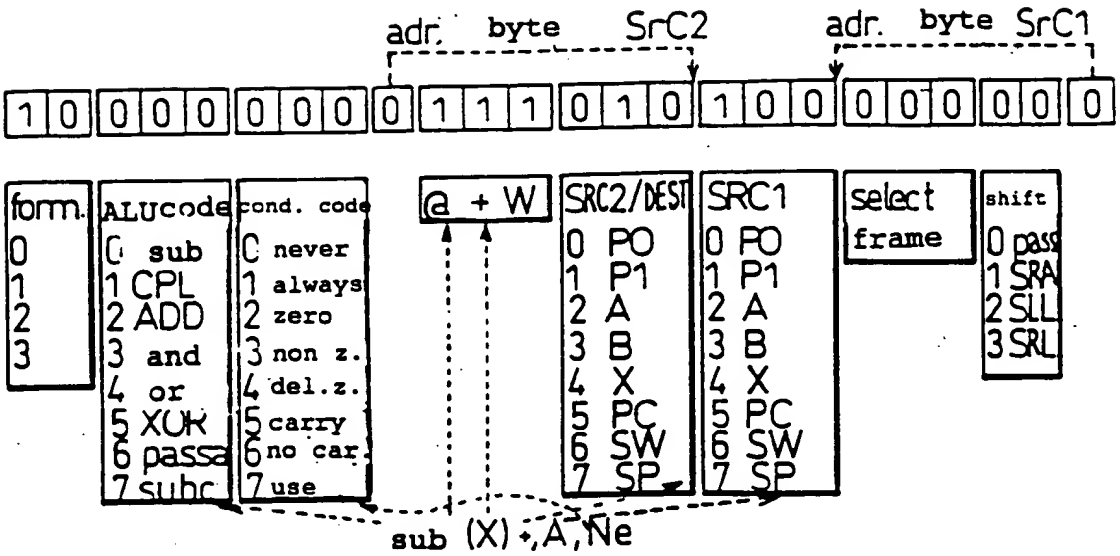
0 - DMA/Rn low
1 - DMA/Rn high

FIG·12

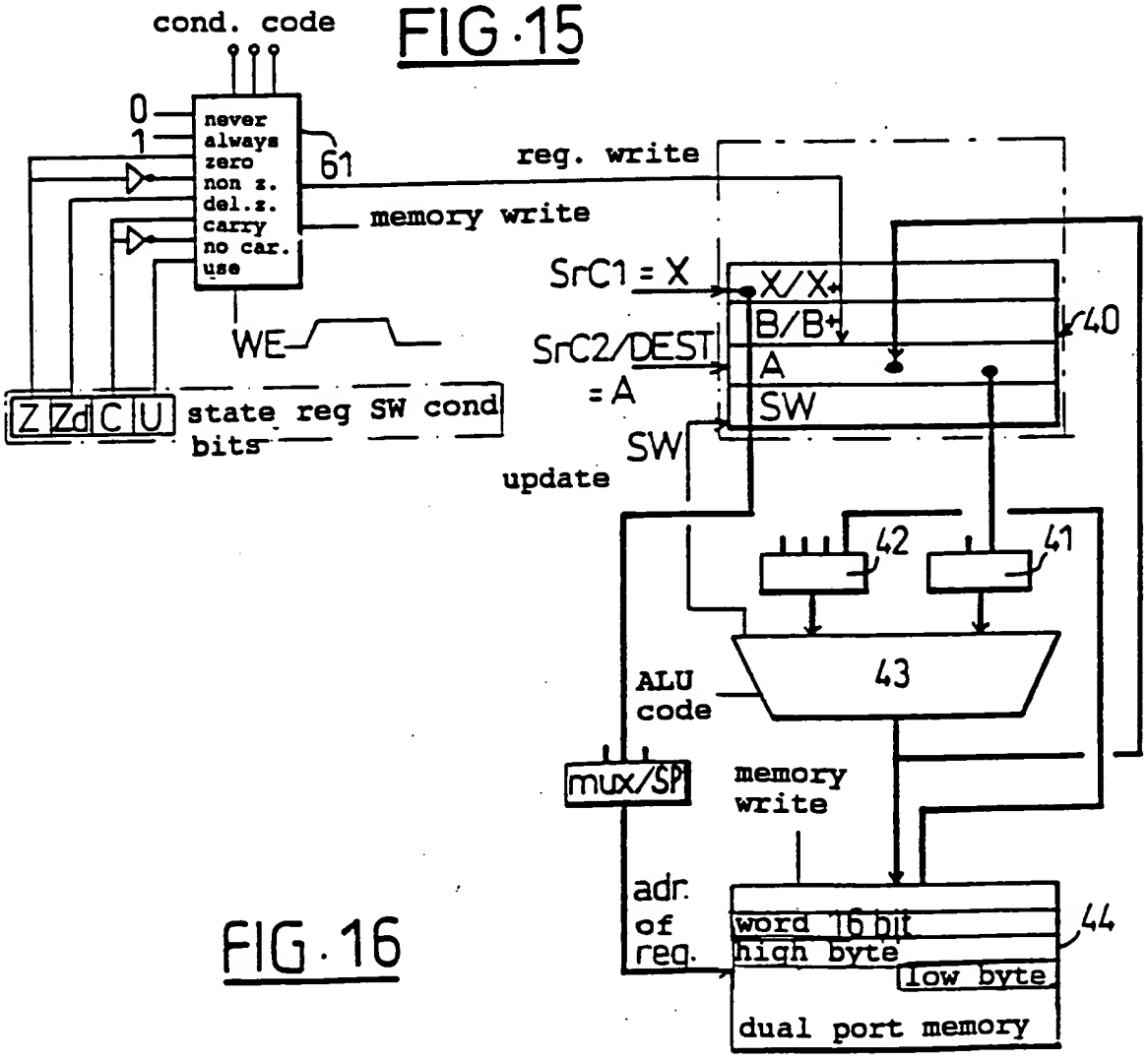

frame 0
SRC1/DEST
select.
periph. reg. P1
periph. reg. P0
Peripherals
Write
Increment/X reg.
40a
Increment/B reg.
40b
40
SRC1 SRC2 & DEST
reg. A
40c
60
state reg. SW
40d
42
41
37
43
39
word 16 bits
44
high byte
low byte
62
61
never
always
zero
non zero
write reg.
delay zer
carry
memory write
no car.
user
WE
state reg. SW cond bits:

FIG·13

FIG·14


adr. byte SrC2
adr. byte SrC1
1 0 0 0 0 0 0 0 0 1 1 1 0 1 0 1 0 0 0 0 0 0 0 0
form.
0
1
2
3
ALUcode
0 sub
1 CPL
2 ADD
3 and
4 or
5 XOR
6 passa
7 subc
cond. code
0 never
1 always
2 zero
3 non z.
4 del.z.
5 carry
6 no car.
7 use
@ + W
SRC2/DEST
0 PO
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
SRC1
0 PO
1 P1
2 A
3 B
4 X
5 PC
6 SW
7 SP
select frame
shift
0 pass
1 SRA
2 SLL
3 SRL
sub (X) +,A,Ne

FIG·15


cond. code
0
1
never
always
zero
non z.
del.z.
carry
no car.
use
61
reg. write
memory write
WE
Z Zd C U
state reg SW cond bits
SrC1 = X
SrC2/DEST = A
X/X+
B/B+
A
SW
40
SW update
42
41
43
ALU code
mux/SP
memory write
adr. of reg.
word 16 bit
high byte
low byte
44
dual port memory

FIG·16

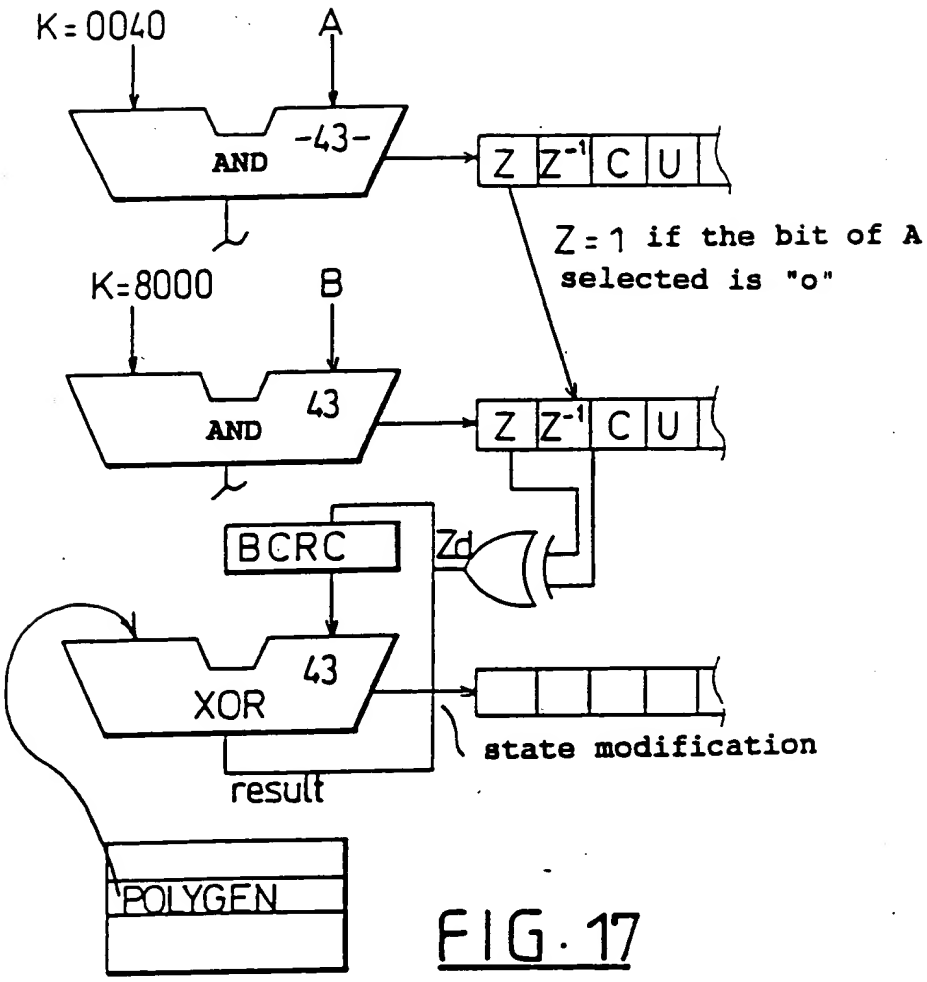


FIG. 17